PCB DESIGN AND VERIFICATION FLOW (FOR DDR-IF)

FLOW GUIDELINE (FOR CUSTOMER)

MARCH.2023 (REV1.0)

MPU BUSINESS DEVELOPMENT DEPARTMENT ENTERPRISE INFRASTRUCTURE BUSINESS DIVISION IOT & INFRASTRUCTURE BUSINESS UNIT RENESAS ELECTRONICS COOPERATION



PCB DESIGN PHASE FOR DDR-IF PART

HOW TO USE HW DESIGN GUIDE AND MODEL Items to be referenced :From 3rd party :From Renesas Start **Check List for Designing** Confirm points to note in advance with the **Circuit Boards** board checklist PCB design guideline for Select Topology with PCB Design Guide DDR4/DDR3L Start PCB design using reference board design data, etc. **Board Design Data** (.dsn, .brd, BOM) No Confirm to satisfies the PCB verification guide for board design checklist DDR4/DDR3L **DDR Memory's models** MPU's models Execute transmission line delay simulation using **IBIS IO Buffer IBIS IO Buffer IBIS** model model model **PKG** model PKG model Confirm that JEDEC (DDR-IF.PDN) No (DDR-IF,PDN) standards and verification guides are satisfied [Important point] If the DDR memory is changed, it is necessary to run the simulation again. Even with the same memory vendor, re-simulation is necessary for products that change. End (This is because the internal memory structure and PKG LCR change.)

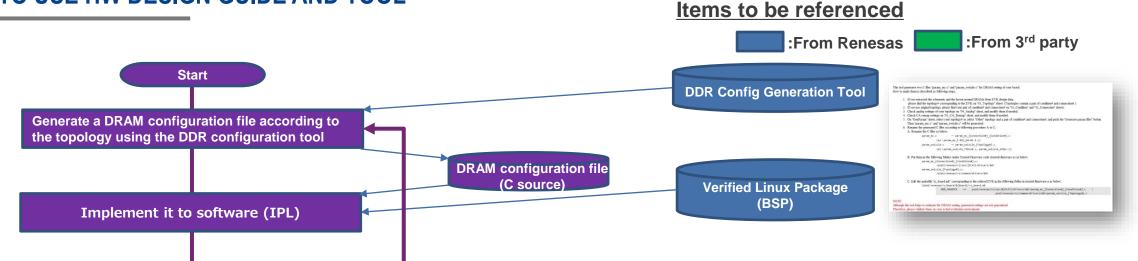
<u>Custom board trial production started → Operation check after completing the board(See next page)</u>



OPERATION CHECK OF CUSTOM BOARD FOR DDR-IF PART

No

HOW TO USE HW DESIGN GUIDE AND TOOL



Upload the software on the custom board, Check operation with custom board

Normal operation, stable operation

End

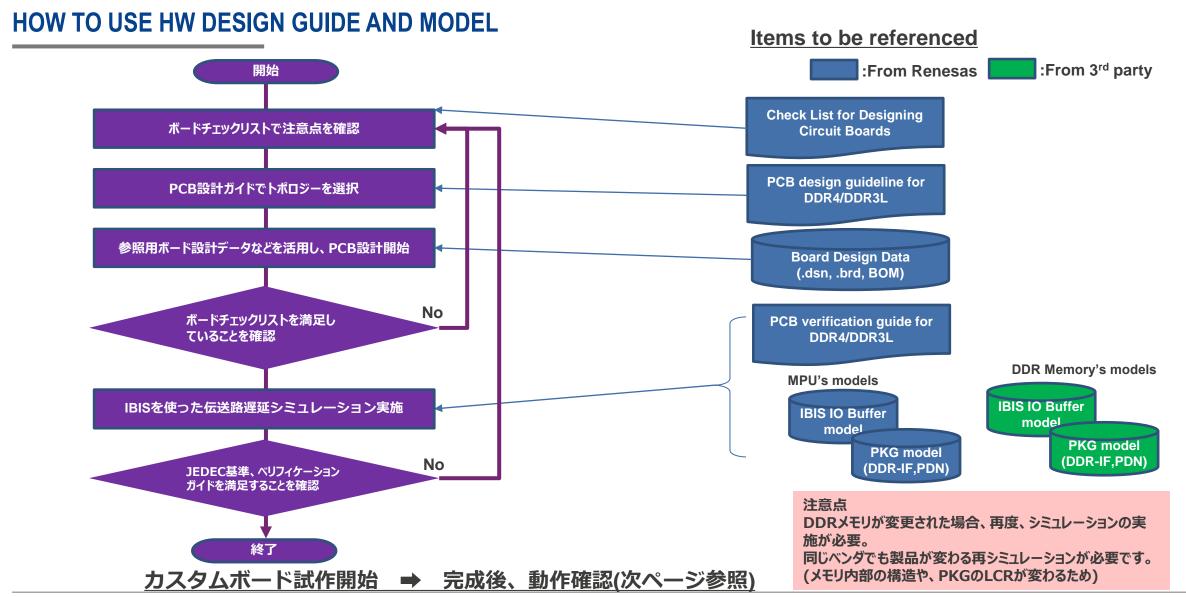
Complete the operation check of the custom board

There are various causes for normal operation and unstable operation. Renesas has prepared guidelines to facilitate the development of boards that operate normally and stably, but they are not perfect. Ultimately, it is the customer's responsibility to identify the cause and implement countermeasures.

- << Reference when you have trouble with board development >>
- Review the settings of the DDR config tool (whether the driving force and topology selection are correct)
- Refer FAQ of board development
- Confirmation of eye-opening status by DQ Margin checker
 (However, DDRPHY calibration cannot be performed manually.
 So you can't adjust the PHY as a countermeasure,
 you have to remove the board issue.)



PCB DESIGN PHASE FOR DDR-IF PART



OPERATION CHECK OF CUSTOM BOARD FOR DDR-IF PART

HOW TO USE HW DESIGN GUIDE AND TOOL

開始

DDRコンフィグツールを用いて、トポロジーに応じたDRAM 設定ファイルを生成

ソフトウエア(IPL)にDRAM設定ファイルを組み込む

Items to be referenced



DRAM設定ファイル (C source)

Verified Linux Package (BSP)

ソフトウエアをカスタムボード上にUploadし、 カスタムボードで動作を確認

No

正常動作、安定動作する

カスタムボード動作確認完了

正常動作、安定動作しない場合の原因はそれぞれあります。 ルネサスでは正常動作、安定動作するボード開発を容易に するためのガイドラインを準備しておりますが、これらは完璧 ではありません。最終的にはお客様にて原因特定、対策を 実施いただく必要があります。

(ボード開発で困ったときの参考)

- ・DDR config toolの設定見直し(駆動力、トポロジー選択が間違っていないか)
- ・ボード開発のFAQを参照
- ・DQ Margin checkerによるEye開口状況の確認 (ただし、DDRPHYのCalibrationはManualでは実行できません。そのため、対策と してPHYを調整することはできないため、ボードの問題を取り除く必要があります。)

Renesas.com